

Sean William Carroll

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Skills

Programming Tools	Modern C++, Python, Rust, SystemVerilog/UVM, Haskell
Deep Learning Frameworks	git, cmake, gdb, valgrind, svn, vcs, dve, verdi, bazel, perforce
Python Libraries	TensorFlow, PyTorch
	pandas, numpy, duckdb, dash, dask, PyQt

Experience

AMD | Aug. 2022 - Present

Boxborough, MA

SMTS SILICON DESIGN ENGINEER | JUL. 2025 - PRESENT

MTS SILICON DESIGN ENGINEER | AUG. 2022 - JUL. 2025

- Architecting and maintaining a cycle-level performance modeling framework in C++11 used to identify throughput ceilings, queuing bottlenecks, and latency-bound behavior in next-generation IO coprocessors
- Designing and implementing a data collection library in modern C++ and Rust for aggregating simulation telemetry, enabling rapid iteration on performance hypotheses across modeling campaigns
- Building new coprocessor simulation modules in C++11 while refactoring shared infrastructure for composability and reduction of technical debt across the modeling codebase
- Leading analytical case studies that synthesize simulation data into architectural recommendations for hardware designers; two papers accepted to internal conference on modeling methodology improvements
- Developing analysis and visualization tooling using pandas, DuckDB, and Plotly to surface performance regressions and validate model predictions against RTL

Redpoint Positioning Corporation | Jan. 2022 - Aug. 2022

Boston, MA

ALGORITHM ENGINEER

- Built a deployment configuration tool in Python (pandas, NumPy, PyQt) that reduced RTLS site deployment time
- Developed a real-time operational dashboard (pandas, NumPy, Dask, Dash) for monitoring deployment health across production RTLS installations
- Created a shared Python package with a reusable API client, unifying common utilities across the R&D team
- Introduced CI pipelines with linting and test stages for three projects, establishing the team's first automated quality gates

Apple | Aug. 2021 - Jan. 2022

Cambridge, MA

DESIGN VERIFICATION ENGINEER FOR ANALOG/MIXED SIGNAL GROUP

- Developed SystemVerilog assertion-based verification for a firmware-driven analog/mixed-signal component

Lightelligence | Nov. 2019 - Aug. 2021

Boston, MA

COMPUTER ARCHITECT | MAR. 2020 - AUG. 2021

- Designed and implemented a microarchitectural simulator from scratch in modern C++ (event-driven, object-oriented) with a Python front end, used as the primary tool for architecture exploration and performance validation
- Co-designed the microarchitecture of a linear algebra accelerator for ML workloads, featuring a novel photonic network-on-chip interconnect
- Grew the architecture team from 1 to 4 engineers through technical interviews and hiring

DESIGN VERIFICATION ENGINEER | NOV. 2019 - MAR. 2020

- Built an extensible Python code generation framework that consumed SystemRDL register descriptions and produced RTL, verification, and C driver collateral, eliminating manual boilerplate across the design team
- Bootstrapped and owned the gate-level simulation flow for Lightelligence's first test chip

Marvell Semiconductor (formerly Cavium) | Sep. 2017 - Nov. 2019

Marlborough, MA

DESIGN VERIFICATION ENGINEER

- Co-authored a lightweight OS framework and test suite in C and SystemVerilog for full-chip integration verification of SOC coprocessors
- Contributed features to an internal Python linting tool, reducing debug loop time by catching common errors earlier in the workflow
- Mentored a college intern through delivery of a report aggregation tool that eliminated manual collation of test results

Education

Georgia Institute of Technology

Atlanta, GA

M.S. IN COMPUTER SCIENCE

Jan. 2018 - May 2021

- OMSCS (Remote) · GPA: 4.0 · Machine Learning Specialization

Cornell University

Ithaca, NY

B.S. IN COMPUTER SCIENCE, ELECTRICAL AND COMPUTER ENGINEERING

Aug. 2013 - May 2017

- GPA: 3.871 (*Magna Cum Laude*), Dean's List (All Semesters) · Systems/Databases Vector (OS Track)